AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

1. (Currently Amended) A circuit substrate comprising:

a first substrate on a first surface of which circuit elements are loaded;

a second substrate on which the first substrate is loaded; and

noise reduction elements each sandwiched between an area of a second surface of the first substrate over against the first surface of the first substrate and a surface of the second substrate facing the second surface of the first substrate, the noise reduction elements each being connected between a power source terminal of the second surface of the first substrate and a power source terminal of the surface of the second substrate, wherein the power source terminal of the first substrate is electrically connected to a power source line of the second substrate through a via.

2. (Original) A circuit substrate according to claim 1, wherein the noise reduction element is a chip condenser.

3. (Original) A circuit substrate according to claim 1, wherein a signal terminal of the second surface of the first substrate is connected with a signal terminal of the surface of the second substrate in accordance with a ball grid array system.

4. (Original) A circuit substrate according to claim 2, wherein a signal terminal of the second surface of the first substrate is connected with a signal terminal of the surface of the second substrate in accordance with a ball grid array system.

5. (Currently Amended) Electronic equipment on which a circuit substrate is loaded, the electronic equipment being operative in accordance with an electronic circuit constructed on the circuit substrate, wherein the circuit substrate comprises:

a first substrate on a first surface of which circuit elements are loaded;

a second substrate on which the first substrate is loaded; and

noise reduction elements each sandwiched between an area of a second surface of the first substrate over against the first surface of the first substrate and a surface of the second substrate facing the second surface of the first substrate, the noise reduction elements each being connected between a power source terminal of the second surface of the first substrate and a power source terminal of the surface of the second substrate, wherein the power source terminal of the first substrate is electrically connected to a power source line of the second substrate through a via.

6. (Original) Electronic equipment according to claim 5, wherein the noise reduction element is a chip condenser.

7. (Original) Electronic equipment according to claim 5, wherein a signal terminal of the second surface of the first substrate is connected with a signal terminal of the surface of the second substrate in accordance with a ball grid array system.

8. (Original) Electronic equipment according to claim 6, wherein a signal terminal of the second surface of the first substrate is connected with a signal terminal of the surface of the second substrate in accordance with a ball grid array system.

9. (Previously Presented) A circuit substrate according to claim 1, wherein the noise reduction elements are each connected between a ground terminal of the second surface of the first substrate and a ground terminal of the surface of the second substrate.

10. (Previously Presented) A circuit substrate according to claim 5, wherein the noise reduction elements are each connected between a ground terminal of the second surface of the first substrate and a ground terminal of the surface of the second substrate.